AMENDMENTS TO THE CLAIMS

1. (**Currently amended**) A method for parametrizing an integrated circuit with a supply voltage terminal~~, a reference potential terminal~~ and an output terminal, comprising:

applying to ~~at least one of~~ the supply voltage terminal ~~and the output terminal~~ a digital start command signal followed by a parametrization data signal; and

detecting the start command signal with a detecting device located in the integrated circuit, wherein a voltage level that is higher than a normal operating voltage level of the integrated circuit, is applied continuously during parametrization to the supply voltage terminal ~~and output terminal~~.

2. (Original) The method of claim 1, wherein the parametrization data signal includes a code having a plurality of bits and wherein after each bit an edge thereof is changed.

3. (Original) The method of claim 2, wherein a first logical state of a bit is determined by an additional edge change approximately in the middle of a bit length and a second logical state of a bit is determined by a signal that remains constant during the bit length.

4. (Original) The method of claim 2, wherein the integrated circuit further includes an oscillator and an interface device for processing a predetermined variable clock frequency of the parametrization signal, and wherein a time window is defined at the beginning of each bit and wherein within the duration of the time window an edge change is expected signaling an end of the bit.

5. (Original) The method of claim 4, wherein a time duration of the bit is determined following the occurrence of at least one edge change marking the end of the bit, and wherein the next edge change is expected to be offset by this time duration.

6. (Original) The method of claim 5, wherein the time duration of a bit is determined from the average time duration of at least two consecutive bits.

7. (Original) The method of claim 1, wherein the integrated circuit further includes a non-volatile memory for storing an adjustment specification for adjusting at least one circuit component to be parametrized and wherein the parametrization data activate the adjustment of the circuit component according to the adjustment specification.

8. (Original) The method of claim 1, wherein the output terminal of the integrated circuit supplies a signal confirming the parametrization process.

9. (Original) The method of claim 1, wherein the parametrization process includes a parameter address identifying the integrated circuit.

10. (**Currently amended**) An integrated circuit receiving parametrization data signals for parametrizing the integrated circuit, comprising:

a supply voltage terminal~~, a reference potential terminal,~~and an output terminal, ~~at least one of~~ the supply voltage terminal ~~and the output terminal~~ receiving a digital start command signal followed by a parametrization data signal;

an oscillator;

a storage device;

an interface device connected to the oscillator, the output terminal and the storage device; and

a detecting device connected between the supply voltage terminal and the interface device for detecting the start command signal, wherein a voltage level that is applied continuously during parametrization to the supply voltage terminal ~~and~~

~~output terminal~~ is higher than a normal operating voltage level of the integrated circuit.

11. (Original) The integrated circuit of claim 10, further comprising:

an analog circuit section connected to the storage device, wherein the analog circuit section is adjusted in accordance with the parametrization data signal.

12. (Original) The integrated circuit of claim 10, wherein the detecting device has a threshold voltage of approximately + 5V.

13. (Original) The integrated circuit of claim 10, wherein the storage device is a non-volatile storage device.

14. (Original) The integrated circuit of claim 10, wherein the integrated circuit comprises at least one sensor.

15. (Original) The integrated circuit of claim 10, wherein the parametrization data signal is defined by a sync bit followed by command bits, address bits, and data bits.

16. (Original) The integrated circuit of claim 15, wherein the sync bit is followed by four command bits, four address bits, and twelve data bits.

17. (Original) The integrated circuit of claim 14, wherein the sensor is a Hall sensor.

18. (**Currently amended**) A method for parametrizing an integrated circuit, comprising:

applying <u>to a supply voltage terminal of the integrated circuit a parametrization signal, the parametrization signal comprising</u> a continuous voltage level that is higher than a normal operating voltage level of the integrated circuit to <u>the</u>~~a~~ supply voltage terminal ~~and an output terminal~~ of the integrated circuit~~; and~~

~~applying a parametrization signal to at least one of the supply voltage terminal and the output terminal~~.

19. (**Currently amended**) An integrated circuit, comprising:

a plurality of terminals receiving operating voltage levels to operate the integrated circuit, the plurality of terminals including a supply voltage terminal; and

means for parametrizing the integrated circuit by continuously applying to ~~at least two of the terminals~~ the supply voltage terminal a voltage level that is higher than the normal operating voltage levels of the integrated circuit, during the presence of a parametrization signal.

20. (Original) The integrated circuit of claim 19, wherein a number of terminals for parametrizing the integrated circuit is no greater than a number of terminals required to operate the integrated circuit.

21. (**Currently amended**) A system for parametrizing an integrated circuit, comprising:

a control device that defines functions of the integrated circuit to be parametrized; and

a protocol generator, coupled to the control device, that receives the defined functions from the control device and converts the functions into parametrization signals, wherein the protocol generator is connected to a supply voltage terminal, ~~a reference potential terminal and an output terminal of the integrated circuit~~ and wherein the integrated circuit is parametrized by continuously applying to the supply voltage terminal ~~and the output terminal~~ a voltage level that is higher than the normal operating voltage levels of the integrated circuit, during the presence of the parametrization signal.